

SEMITOP[®] 2

Antiparallel Thyristor Module

SK 100 KQ

Preliminary Data

Features

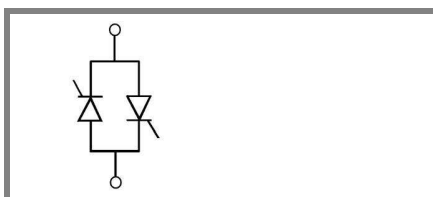
- Compact Design
- One screw mounting
- Heat transfer and isolation through direct copper bonded aluminium oxide ceramic (DBC)
- Glass passivated thyristor chips
- Up to 1600V reverse voltage
- UL recognized, file no. E 63 532

Typical Applications

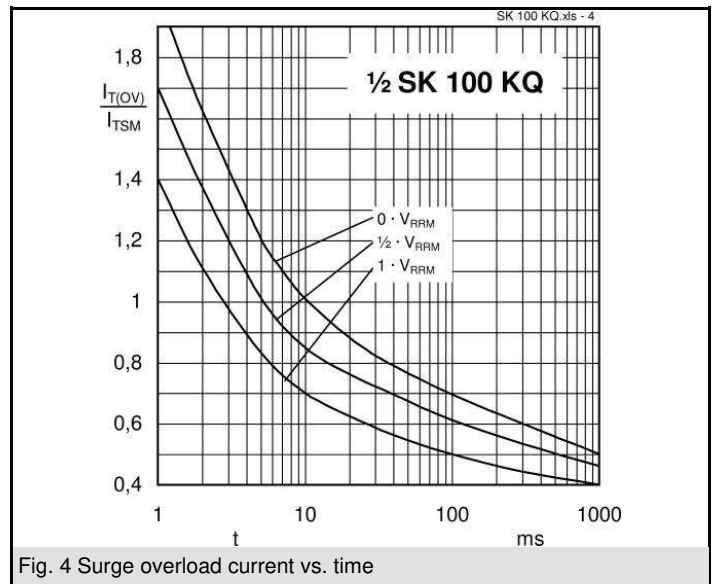
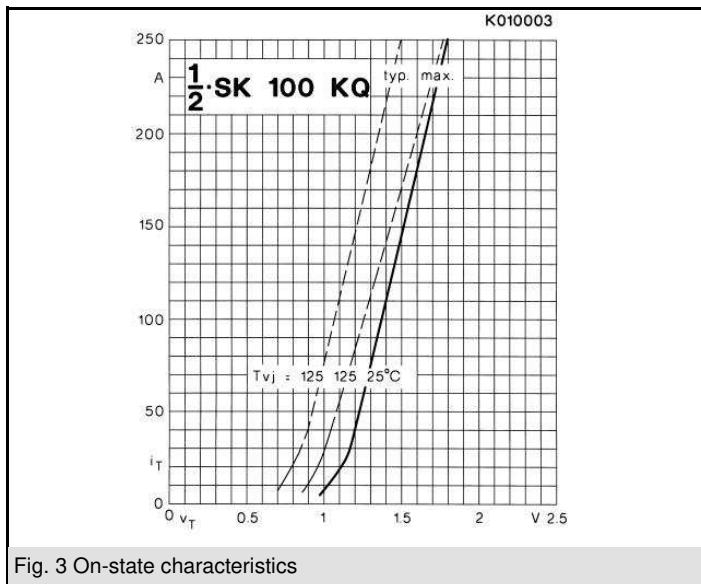
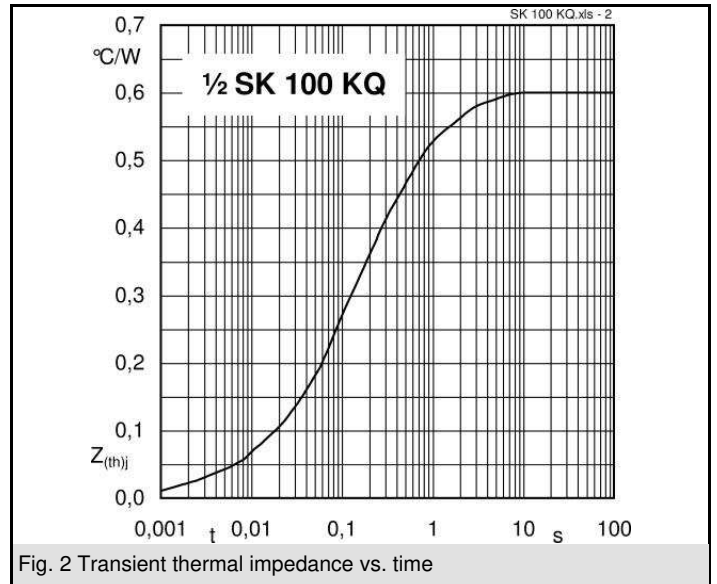
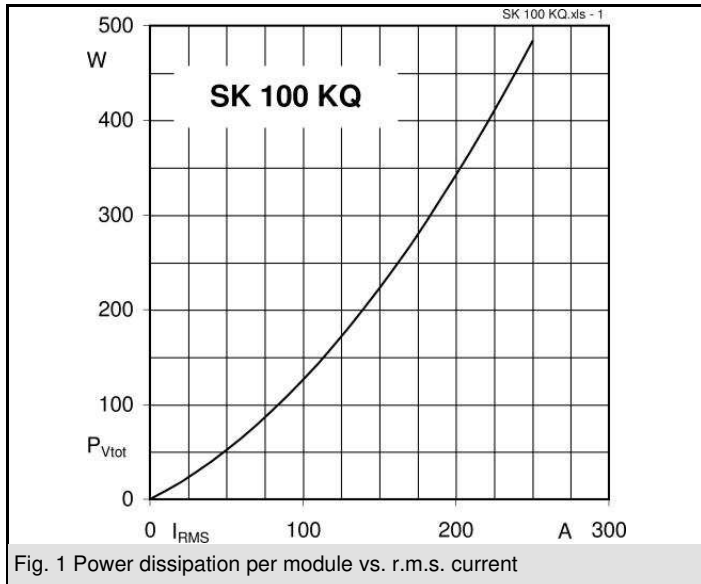
- Soft starters
- Light control (studios, theaters...)
- Temperature control

V_{RSM} V	V_{RRM}, V_{DRM} V	$I_{RMS} = 101$ A (full conduction) ($T_s = 85$ °C)
900	800	SK 100 KQ 08
1300	1200	SK 100 KQ 12
1700	1600	SK 100 KQ 16

Symbol	Conditions	Values	Units
I_{RMS}	W1C ; sin. 180° ; $T_s = 100$ °C	71	A
	W1C ; sin. 180° ; $T_s = 85$ °C	101	A
I_{TSM}	$T_{vj} = 25$ °C ; 10 ms	1500	A
	$T_{vj} = 125$ °C ; 10 ms	1350	A
i^2t	$T_{vj} = 25$ °C ; 8,3...10 ms	11250	A ² s
	$T_{vj} = 125$ °C ; 8,3...10 ms	9100	A ² s
V_T	$T_{vj} = 25$ °C, $I_T = 200$ A	max. 1,8	V
$V_{T(TO)}$	$T_{vj} = 125$ °C	max. 0,9	V
r_T	$T_{vj} = 125$ °C	max. 4,5	mΩ
I_{DD}, I_{RD}	$T_{vj} = 25$ °C, $V_{RD} = V_{RRM}$	max. 1	mA
	$T_{vj} = 125$ °C, $V_{RD} = V_{RRM}$	max. 20	mA
t_{gd}	$T_{vj} = 25$ °C, $I_G = 1$ A; $di_G/dt = 1$ A/μs	1	μs
t_{gr}	$V_D = 0,67 * V_{DRM}$	2	μs
$(dv/dt)_{cr}$	$T_{vj} = 125$ °C	1000	V/μs
$(di/dt)_{cr}$	$T_{vj} = 125$ °C; $f = 50...60$ Hz	100	A/μs
t_q	$T_{vj} = 125$ °C; typ.	80	μs
I_H	$T_{vj} = 25$ °C; typ. / max.	100 / 200	mA
I_L	$T_{vj} = 25$ °C; $R_G = 33$ Ω; typ. / max.	200 / 500	mA
V_{GT}	$T_{vj} = 25$ °C; d.c.	min. 2	V
I_{GT}	$T_{vj} = 25$ °C; d.c.	min. 100	mA
V_{GD}	$T_{vj} = 125$ °C; d.c.	max. 0,25	V
I_{GD}	$T_{vj} = 125$ °C; d.c.	max. 5	mA
$R_{th(j-s)}$	cont. per thyristor	0,6	K/W
	sin 180° per thyristor	0,63	K/W
$R_{th(j-s)}$	cont. per W1C	0,3	K/W
	sin 180° per W1C	0,315	K/W
T_{vj}		-40 ... +125	°C
T_{stg}		-40 ... +125	°C
T_{solder}	terminals, 10s	260	°C
V_{isol}	a. c. 50 Hz; r.m.s.; 1 s / 1 min.	3000 / 2500	V~
M_s	Mounting torque to heatsink	2,0	Nm
M_t			Nm
a			m/s ²
m		19	g
Case	SEMITOP [®] 2	T 2	



KQ



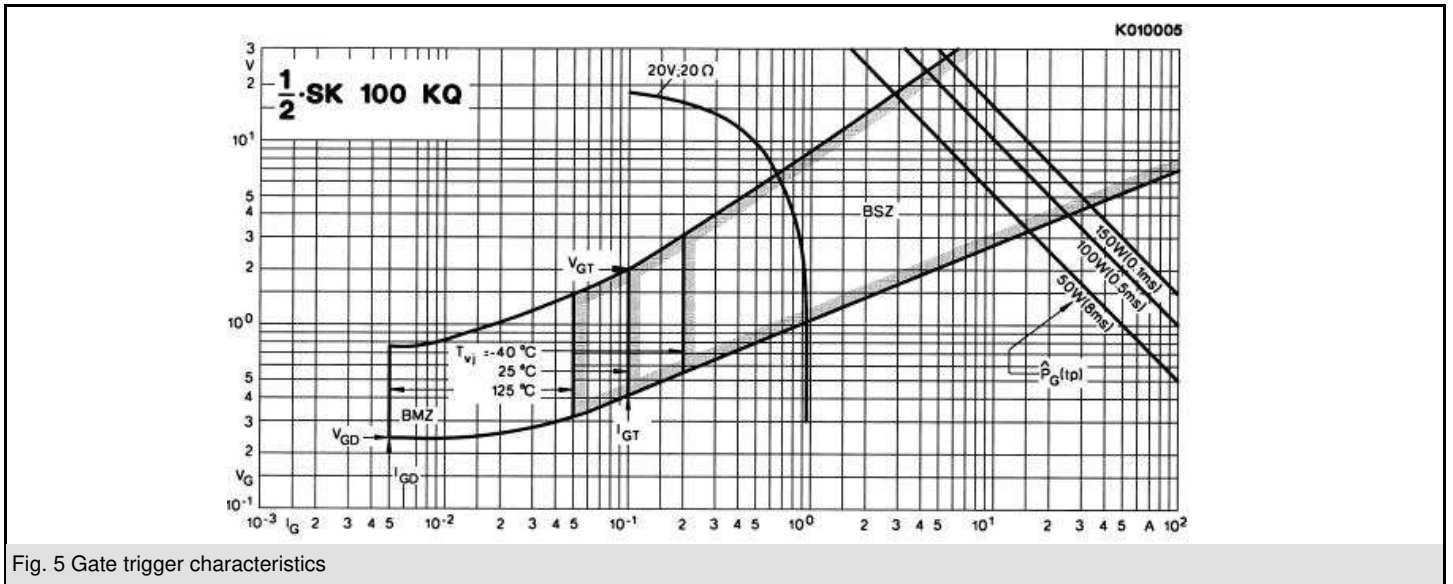
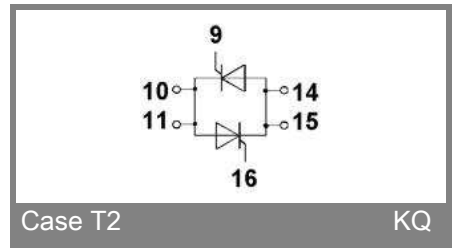
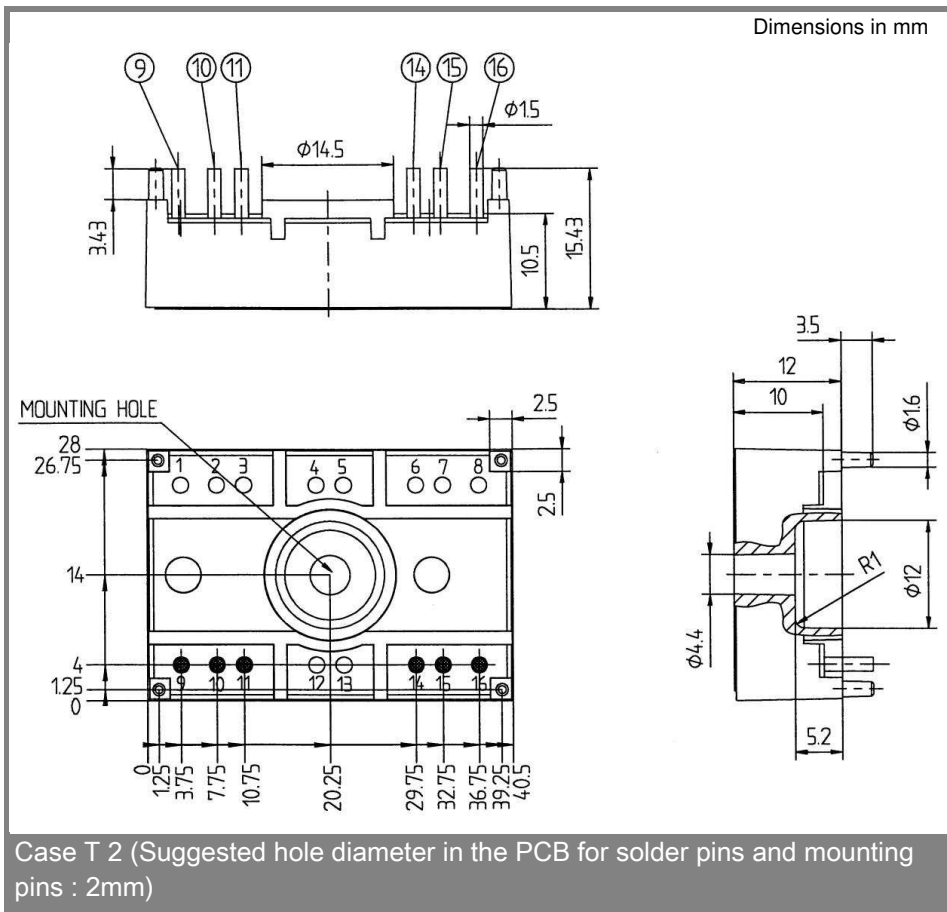


Fig. 5 Gate trigger characteristics



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